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a second plate attached to the first plate for retaining the die therebetween; and

a plastic film placed between the first plate and the second plate for electrically connecting the die to test circuitry, the film comprising a bump for physically and electrically contacting a contact on the die, a conductive trace in electrical communication with the bump, and an electrical connector in electrical communication with the trace and connectable to the test circuitry;

with the connector, and at least a portion of the trace extending beyond a confine of the fixture, and with the bump, the trace, and the connector configured to provide a direct electrical path from the test circuitry to the contact on the die.

35. (added) The fixture of claim 34 wherein the plastic film comprises polyimide.

36. (added) The fixture of claim 34 wherein the first plate comprises a die receiving cavity sized to receive the die.

37. (added) The fixture of claim 34 further comprising an elastomeric biasing member placed between the first plate and the second plate for biasing the bump against the contact.

38. (added) The fixture of claim 34 further comprising a clamp for securing the first plate to the second plate.

39. (added) A test fixture for testing a semiconductor die comprising:

a first plate for receiving the die;
a second plate attached to the first plate for retaining the die on the first plate; and

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a plastic film for electrically connecting the die to test circuitry, the film comprising a bump for physically and electrically contacting a contact on the die, a conductive trace in electrical communication with the bump, and an electrical connector in electrical communication with the trace and connectable to the test circuitry;

with a first portion of the film placed between the first plate and the second plate and biased against the die;

with a second portion of the film and the connector extending beyond a confine of the fixture, and with the bump, the trace and the connector providing a direct electrical path from the test circuitry to the contact on the die.

40. (added) The test fixture of claim 39 further comprising a compressible elastomeric pad placed between the first plate and the second plate to bias the first portion of the film against the die.

41. (added) The test fixture of claim 39 wherein the film comprise polyimide and the bump comprises solder.

42. (added) The test package of claim 39 wherein the film comprise polyimide and the bump comprises a conductive polymer.

43. (added) A test fixture for testing a semiconductor die comprising:

a first plate for receiving the die;

a second plate attached to the first plate for retaining the die on the first plate; and

a plastic film for electrically connecting the die to test circuitry, the film comprising a bump for physically and electrically contacting a contact on the die, a conductive trace in electrical communication with the bump, and an electrical connector in electrical communication with the trace and connectable to the test circuitry;

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a compressible elastomeric pad placed between the first plate and the second plate for biasing the bump against the contact;

with a first portion of the film placed between the first plate and the second plate and biased against the die by the pad;

with a second portion of the film and the connector extending beyond a confine of the fixture, and with the bump, the trace, and the connector providing an electrical path independent of the first plate and the second plate, from the test circuitry to the contact on the die.

44. (added) The test fixture of claim 43 wherein the bump comprises a material selected from the group consisting of metal and a conductive polymer.

45. (added) The test fixture of claim 43 wherein the first plate includes a cavity for retaining the die.

46. (added) The test fixture of claim 43 wherein the first plate includes a cavity and a spacer member within the cavity for retaining the die.

47. (added) A method for testing a semiconductor die comprising:

providing a test circuitry configured to generate test signals;

providing a test fixture comprising a first plate and a second plate configured to house the die;

providing a die contact member between the first plate and the second plate for electrically connecting the die to the test circuitry, the die contact member comprising a plastic film, a bump on the film for electrically contacting a contact on the die, a conductive trace on the film in electrical communication with the bump for conducting the test signals to the bump, and an electrical connector on

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the film in electrical communication with the trace configured for electrical connection to the test circuitry, the trace extending continuously on the film from the connector to the bump and with the connector, the trace and the bump providing a direct electrical path from the test circuitry to the contact;

providing a compressible member configured for placement between the first plate and the second plate to bias the die against the die contact member;

placing the die on the first plate with the contact on the die in physical and electrical contact with the bump;

securing the second plate to the first plate with the compressible member compressed therebetween to bias the bump against the contact and with the connector, and at least a portion of the film and the trace extending outside the first plate and the second plate; and

electrically connecting the connector to the test circuitry.

48. (added) The method of claim 47 wherein the first plate comprises a die receiving cavity sized to retain the die.

49. (added) The method of claim 47 wherein the contact on the die comprises a bond pad.

50. (added) A method for testing a semiconductor die comprising:

providing a test circuitry configured to generate test signals;

providing a test fixture comprising a first plate and a second plate configured to house the die in electrical communication with the test circuitry;

providing a die contact member configured for placement between the first plate and the second plate for electrically connecting the die to the test circuitry, the

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die contact member comprising a polyimide film, a bump on the film for electrically contacting a contact on the die, a conductive trace on the film in electrical communication with the bump for conducting the test signals to the bump, and an electrical connector on the film in electrical communication with the trace configured for electrical connection to the test circuitry, the trace extending continuously on the film from the connector to the bump and with the connector, the trace and the bump providing a direct electrical path from the test circuitry to the contact;

providing a compressible member configured for placement between the first plate and the second plate to bias the die against the die contact member;

placing the die on the first plate with the contact on the die in direct electrical contact with the bump;

securing the second plate to the first plate with the compressible member compressed therebetween to bias the bump against the contact and with the connector, and at least a portion of the film and the trace extending outside the first plate and the second plate; and

applying the test signals through the die contact member to the die.

51. (added) The method of claim 50 wherein the bump comprises a conductive polymer.

52. (added) A method for testing a semiconductor die comprising:

providing a test circuitry configured to generate test signals;

providing a test fixture comprising a first plate and a second plate configured to house the die;

providing a die contact member configured for placement between the first plate and the second plate to electrically connect the die to the test circuitry, the die contact member comprising a plastic film, a bump on the film

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